What is claimed is:

1. A method for designing a device or system capable of:
implementing a hash algorithm which can generate the hash of an input message block using only non-sequential structures and logic elements which perform the plurality of the intermediate stage computations and logical operations of a hash algorithm without the use of a clock;

2. A device or system using the methodology of claim **1** capable of;
generating the full hash of an N-block long message in no more than N-process (clocks) cycles.

3. A device or system using the methodology of claim **1** wherein;
the total propagation delay through a critical delay path specifies the speed of a system or device.

4. An apparatus built using the methodology of claim **1** wherein:
a system or device manifested in an implementing technology is the physical expression of the design methodology of such a system or device.

5. An apparatus as claimed in claim **4**;
can be built to implement any hash algorithm.